LatticeECP2/M Family Data Sheet
Introduction

Features

■ **High Logic Density for System Integration**
  - 6K to 95K LUTs
  - 90 to 583 I/Os

■ **Embedded SERDES (LatticeECP2M Only)**
  - Data Rates 250 Mbps to 3.125 Gbps
  - Up to 16 channels per device
    PCI Express, Ethernet (1GbE, SGMII), OBSAI, CPRI and Serial RapidIO.

■ **sysDSP™ Block**
  - 3 to 42 blocks for high performance multiply and accumulate
  - Each block supports
    – One 36x36, four 18X18 or eight 9X9 multipliers

■ **Flexible Memory Resources**
  - 55Kbits to 5308Kbits sysMEM™ Embedded Block RAM (EBR)
    – 18Kbit block
    – Single, pseudo dual and true dual port
    – Byte Enable Mode support
  - 12K to 202Kbits distributed RAM
    – Single port and pseudo dual port

■ **sysCLOCK Analog PLLs and DLLs**
  - Two GPLLs and up to six SPLLs per device
    – Clock multiply, divide, phase & delay adjust
    – Dynamic PLL adjustment
  - Two general purpose DLLs per device

■ **Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
  - Dedicated gearing logic
  - Source synchronous standards support
    – SPI4.2, SFI4 (DDR Mode), XGMII
    – High Speed ADC/DAC devices
  - Dedicated DDR and DDR2 memory support
    – DDR1: 400 (200MHz) / DDR2: 533 (266MHz)
  - Dedicated DQS support

■ **Programmable sysI/O™ Buffer Supports Wide Range Of Interfaces**
  - LVTTL and LVCMOS 33/25/18/15/12
  - SSTL 3/2/18 I, II
  - HSTL15 I and HSTL18 I, II
  - PCI and Differential HSTL, SSTL
  - LVDS, RSDS, Bus-LVDS, MLVDS, LVPECL

■ **Flexible Device Configuration**
  - 1149.1 Boundary Scan compliant
  - Dedicated bank for configuration I/Os
  - SPI boot flash interface
  - Dual boot images supported
  - TransFR™ I/O for simple field updates
  - Soft Error Detect macro embedded

■ **Optional Bitstream Encryption (LatticeECP2/M "S" Versions Only)**

■ **System Level Support**
  - ispTRACY™ internal logic analyzer capability
  - On-chip oscillator for initialization & general use
  - 1.2V power supply

Table 1-1. LatticeECP2 (Including "S-Series") Family Selection

Device	ECP2-6	ECP2-12	ECP2-20	ECP2-35	ECP2-50	ECP2-70
LUTs (K)	6	12	21	32	48	68
Distributed RAM (Kbits)	12	24	42	64	96	136
EBR SRAM (Kbits)	55	221	276	332	387	1032
EBR SRAM Blocks	3	12	15	18	21	60
sysDSP Blocks	3	6	7	8	18	22
18x18 Multipliers	12	24	28	32	72	88
GPLL + SPLL + DLL	2+0+2	2+0+2	2+0+2	2+0+2	2+2+2	2+4+2
Maximum Available I/O	190	297	402	450	500	583
Packages and I/O Combinations						
144-pin TQFP (20 x 20 mm)	90	93				
208-pin PQFP (28 x 28 mm)		131	131			
256-ball fpBGA (17 x 17 mm)	190	193	193			
484-ball fpBGA (23 x 23 mm)		297	331	331	339	
672-ball fpBGA (27 x 27 mm)			402	450	500	500
900-ball fpBGA (31 x 31 mm)						583

Table 1-2. LatticeECP2M (Including "S-Series") Family Selection

Device	ECP2M20	ECP2M35	ECP2M50	ECP2M70	ECP2M100
LUTs (K)	19	34	48	67	95
sysMEM Blocks (18kb)	66	114	225	246	288
Embedded Memory (Kbits)	1217	2101	4147	4534	5308
Distributed Memory (Kbits)	41	71	101	145	202
sysDSP Blocks	6	8	22	24	42
18x18 Multipliers	24	32	88	96	168
GPLL+SPLL+DLL	2+6+2	2+6+2	2+6+2	2+6+2	2+6+2
Maximum Available I/O	304	410	410	436	520
Packages and SERDES / I/O Combinations					
256-ball fpBGA (17 x 17 mm)	4 / 140	4 / 140			
484-ball fpBGA (23 x 23 mm)	4 / 304	4 / 303	4 / 270		
672-ball fpBGA (27 x 27 mm)		4 / 410	8 / 372		
900-ball fpBGA (31 x 31 mm)			8 / 410	16 / 416	16 / 416
1152-ball fpBGA (35 x 35 mm)				16 / 436	16 / 520

Introduction

The LatticeECP2/M family of FPGA devices is optimized to deliver high performance features such as advanced DSP blocks, high speed SERDES (LatticeECP2M family only) and high speed source synchronous interfaces in an economical FPGA fabric. This combination was achieved through advances in device architecture and the use of 90nm technology.

The LatticeECP2/M FPGA fabric is optimized with high performance and low cost in mind. The LatticeECP2/M devices include LUT-based logic, distributed and embedded memory, Phase Locked Loops (PLLs), Delay Locked Loops (DLLs), pre-engineered source synchronous I/O support, enhanced sysDSP blocks and advanced configuration support, including encryption ("S" versions only) and dual boot capabilities.

The LatticeECP2M device family features high speed SERDES with PCS. These high jitter tolerance and low transmission jitter SERDES with PCS blocks can be configured to support an array of popular data protocols including PCI Express, Ethernet (1GbE and SGMII), OBSAI and CPRI. Transmit Pre-emphasis and Receive Equalization settings make SERDES suitable for chip to chip and small form factor backplane applications.

The ispLEVER® design tool suite from Lattice allows large complex designs to be efficiently implemented using the LatticeECP2/M FPGA family. Synthesis library support for LatticeECP2/M is available for popular logic synthesis tools. The ispLEVER tool uses the synthesis tool output along with the constraints from its floor planning tools to place and route the design in the LatticeECP2/M device. The ispLEVER tool extracts the timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) ispLeverCORE™ modules for the LatticeECP2/M family. By using these IP cores as standardized blocks, designers are free to concentrate on the unique aspects of their design, increasing their productivity.

LatticeECP2/M Family Data Sheet
DC and Switching Characteristics

Absolute Maximum Ratings[1, 2, 3]

Supply Voltage V_{CC} . . . . -0.5 to 1.32V

Supply Voltage V_{CCAUX} . . . . -0.5 to 3.75V

Supply Voltage V_{CCJ} . . . . -0.5 to 3.75V

Output Supply Voltage V_{CCIO} . . . . -0.5 to 3.75V

Input or I/O Tristate Voltage Applied[4] . . . . . . -0.5 to 3.75V

Storage Temperature (Ambient) . . . . -65 to 150°C

Junction Temperature (Tj) . . . . +125°C

1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice *Thermal Management* document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of -2V to (V_{IHMAX} + 2) volts is permitted for a duration of <20ns.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Units
V_{CC}[1, 4, 5]	Core Supply Voltage	1.14	1.26	V
V_{CCAUX}[1, 3, 4, 5]	Auxiliary Supply Voltage	3.135	3.465	V
V_{CCPLL}	PLL Supply Voltage	1.14	1.26	V
V_{CCIO}[1, 2, 4]	I/O Driver Supply Voltage	1.14	3.465	V
V_{CCJ}[1]	Supply Voltage for IEEE 1149.1 Test Access Port	1.14	3.465	V
t_{JCOM}	Junction Temperature, Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature, Industrial Operation	-40	100	°C
SERDES External Power Supply (For LatticeECP2M Family Only)				
V_{CCIB}	Input Buffer Power Supply (1.2V)	1.14	1.26	V
	Input Buffer Power Supply (1.5V)	1.425	1.575	V
V_{CCOB}	Output Buffer Power Supply (1.2V)	1.14	1.26	V
	Output Buffer Power Supply (1.5V)	1.425	1.575	V
$V_{CCAUX33}$	Termination Resistor Switching Power Supply	3.135	3.465	V
V_{CCRX}[6]	Receive Power Supply	1.14	1.26	V
V_{CCTX}[6]	Transmit Power Supply	1.14	1.26	V
V_{CCP}[6]	PLL and Reference Clock Buffer Power	1.14	1.26	V

1. If V_{CCIO} or V_{CCJ} is set to 1.2V, they must be connected to the same power supply as V_{CC}. If V_{CCIO} or V_{CCJ} is set to 3.3V, they must be connected to the same power supply as V_{CCAUX}. V_{CC} and V_{CCPLL} must be connected to the same power supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCAUX} ramp rate must not exceed 30mV/µs during power-up when transitioning between 0V and 3.3V.
4. For proper power-up configuration, users must ensure that the configuration control signals such as the CFGx, INITN, PROGRAMN and DONE pins are driven to the proper logic levels when the device powers up. The device power-up is triggered by the last of V_{CC}, V_{CCAUX} or V_{CCIO8} supplies that reaches its minimum valid levels. Alternatively, if the configuration control signals are pulled up by V_{CCIO8}, the V_{CCIO8} (configuration I/O bank) voltage must be powered up prior to or at the same time as the last of VCC or VCCAUX reaches its minimum levels.
5. For power-up, V_{CC} must reach its valid minimum value before powering up V_{CCAUX} (LatticeECP2/M "S" version devices only).
6. V_{CCRX},V_{CCTX} and V_{CCP} must be tied together in each quad and all quads need to be powered up.

Hot Socketing Specifications[1, 2, 3, 4]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{DK}	Input or I/O leakage current	$0 \leq V_{IN} \leq V_{IH}$ (MAX.)	—	—	+/-1000	µA
I_{HDIN}[5]	SERDES average input current when device is powered down and inputs are driven		—	—	4	mA

1. V_{CC}, V_{CCAUX} and V_{CCIO} should rise/fall monotonically. V_{CC} and V_{CCPLL} must be connected to the same power supply (applies to ECP2-6, ECP2-12 and ECP2-20 only).
2. $0 \leq V_{CC} \leq V_{CC}$ (MAX), $0 \leq V_{CCIO} \leq V_{CCIO}$ (MAX) or $0 \leq V_{CCAUX} \leq V_{CCAUX}$ (MAX).
3. I_{DK} is additive to I_{PU}, I_{PW} or I_{BH}.
4. LVCMOS and LVTTL only.
5. Assumes that the device is powered down with all supplies grounded, both P and N inputs driven by a CML driver with maximum allowed V_{CCIB} of 1.575V, 8b10b data and internal AC coupling.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IL}, I_{IH}[1]	Input or I/O Low Leakage	$0 \leq V_{IN} \leq (V_{CCIO} - 0.2V)$	—	—	10	µA
I_{IH}[1]	Input or I/O High Leakage	$(V_{CCIO} - 0.2V) < V_{IN} \leq 3.6V$	—	—	150	µA
I_{PU}	I/O Active Pull-up Current	$0 \leq V_{IN} \leq 0.7\ V_{CCIO}$	-30	—	-210	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) $\leq V_{IN} \leq V_{IH}$ (MAX)	30	—	210	µA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN} = 0.7\ V_{CCIO}$	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	210	µA
I_{BHHO}	Bus Hold High Overdrive Current	$0 \leq V_{IN} \leq V_{CCIO}$	—	—	-210	µA
V_{BHT}	Bus Hold Trip Points	$0 \leq V_{IN} \leq V_{IH}$ (MAX)	V_{IL} (MAX)	—	V_{IH} (MIN)	V
C1	I/O Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	8	—	pf
C2	Dedicated Input Capacitance[2]	V_{CCIO} = 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, V_{CC} = 1.2V, V_{IO} = 0 to V_{IH} (MAX)	—	6	—	pf

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25°C, f = 1.0MHz.

LatticeECP2 Initialization Supply Current[1, 2, 3, 4]

Over Recommended Operating Conditions

Symbol	Parameter	Device	Typ.[5, 6]	Units
I_{CC}	Core Power Supply Current	ECP2-6	34	mA
		ECP2-12	54	mA
		ECP2-20	82	mA
		ECP2-35	135	mA
		ECP2-50	187	mA
		ECP2-70	267	mA
I_{CCAUX}	Auxiliary Power Supply Current	ECP2-6	30	mA
		ECP2-12	30	mA
		ECP2-20	30	mA
		ECP2-35	30	mA
		ECP2-50	30	mA
		ECP2-70	30	mA
I_{CCGPLL}	GPLL Power Supply Current (per GPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCSPLL}	SPLL Power Supply Current (per SPLL)	ECP2-35, -50, -70 Only	0.5	mA
I_{CCIO}	Bank Power Supply Current (per Bank)	All Devices	3	mA
I_{CCJ}	VCCJ Power Supply Current	All Devices	4	mA

1. Until DONE signal is active.
2. For further information about supply current, please see the list of additional technical documentation at the end of this data sheet.
3. Assumes all outputs are tristated, all inputs are configured as LVCMOS and held at the V_{CCIO} or GND.
4. Frequency 0MHz.
5. $T_J = 25^\circ$C, power supplies at nominal voltage.
6. A specific configuration pattern is used that scales with the size of the device; consists of 75% PFU utilization, 50% EBR, and 25% I/O configuration.

LatticeECP2/M External Switching Characteristics[9]

Over Recommended Operating Conditions

Parameter	Description	Device	-7 Min.	-7 Max.	-6 Min.	-6 Max.	-5 Min.	-5 Max.	Units
General I/O Pin Parameters (using Primary Clock without PLL)[1]									
t_{CO}	Clock to Output - PIO Output Register	LFE2-6	—	3.50	—	3.90	—	4.20	ns
		LFE2-12	—	3.50	—	3.90	—	4.20	ns
		LFE2-20	—	3.50	—	3.90	—	4.20	ns
		LFE2-35	—	3.50	—	3.90	—	4.20	ns
		LFE2-50	—	3.50	—	3.90	—	4.20	ns
		LFE2-70	—	3.70	—	4.10	—	4.40	ns
		LFE2M20	—	3.90	—	4.30	—	4.70	ns
		LFE2M35	—	3.90	—	4.30	—	4.70	ns
		LFE2M50	—	4.50	—	5.00	—	5.40	ns
		LFE2M70	—	4.50	—	5.00	—	5.40	ns
		LFE2M100	—	4.50	—	5.00	—	5.40	ns
t_{SU}	Clock to Data Setup - PIO Input Register	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
t_H	Clock to Data Hold - PIO Input Register	LFE2-6	1.40	—	1.70	—	1.90	—	ns
		LFE2-12	1.40	—	1.70	—	1.90	—	ns
		LFE2-20	1.40	—	1.70	—	1.90	—	ns
		LFE2-35	1.40	—	1.70	—	1.90	—	ns
		LFE2-50	1.40	—	1.70	—	1.90	—	ns
		LFE2-70	1.40	—	1.70	—	1.90	—	ns
		LFE2M20	1.40	—	1.70	—	1.90	—	ns
		LFE2M35	1.40	—	1.70	—	1.90	—	ns
		LFE2M50	1.80	—	2.10	—	2.30	—	ns
		LFE2M70	1.80	—	2.10	—	2.30	—	ns
		LFE2M100	1.80	—	2.10	—	2.30	—	ns

LatticeECP2/M External Switching Characteristics[9] (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7 Min.	-7 Max.	-6 Min.	-6 Max.	-5 Min.	-5 Max.	Units
t_{SU_DEL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFE2-6	1.40	—	1.70	—	1.90	—	ns
		LFE2-12	1.40	—	1.70	—	1.90	—	ns
		LFE2-20	1.40	—	1.70	—	1.90	—	ns
		LFE2-35	1.40	—	1.70	—	1.90	—	ns
		LFE2-50	1.40	—	1.70	—	1.90	—	ns
		LFE2-70	1.40	—	1.70	—	1.90	—	ns
		LFE2M20	1.40	—	1.70	—	1.90	—	ns
		LFE2M35	1.40	—	1.70	—	1.90	—	ns
		LFE2M50	1.40	—	1.70	—	1.90	—	ns
		LFE2M70	1.40	—	1.70	—	1.90	—	ns
		LFE2M100	1.40	—	1.70	—	1.90	—	ns
t_{H_DEL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
f_{MAX_IO}	Clock Frequency of I/O Register and PFU Register	ECP2/M	—	420	—	357	—	311	MHz
General I/O Pin Parameters (using Edge Clock without PLL)[1]									
t_{COE}	Clock to Output - PIO Output Register	LFE2-6	—	2.60	—	2.90	—	3.20	ns
		LFE2-12	—	2.60	—	2.90	—	3.20	ns
		LFE2-20	—	2.60	—	2.90	—	3.20	ns
		LFE2-35	—	2.60	—	2.90	—	3.20	ns
		LFE2-50	—	2.60	—	2.90	—	3.20	ns
		LFE2-70	—	2.60	—	2.90	—	3.20	ns
		LFE2M20	—	2.60	—	2.90	—	3.20	ns
		LFE2M35	—	2.60	—	2.90	—	3.20	ns
		LFE2M50	—	3.10	—	3.40	—	3.70	ns
		LFE2M70	—	3.10	—	3.40	—	3.70	ns
		LFE2M100	—	3.10	—	3.40	—	3.70	ns

LatticeECP2/M External Switching Characteristics[9] (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7 Min.	-7 Max.	-6 Min.	-6 Max.	-5 Min.	-5 Max.	Units
t_{SUE}	Clock to Data Setup - PIO Input Register	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
t_{HE}	Clock to Data Hold - PIO Input Register	LFE2-6	0.90	—	1.10	—	1.30	—	ns
		LFE2-12	0.90	—	1.10	—	1.30	—	ns
		LFE2-20	0.90	—	1.10	—	1.30	—	ns
		LFE2-35	0.90	—	1.10	—	1.30	—	ns
		LFE2-50	0.90	—	1.10	—	1.30	—	ns
		LFE2-70	0.90	—	1.10	—	1.30	—	ns
		LFE2M20	0.90	—	1.10	—	1.30	—	ns
		LFE2M35	0.90	—	1.10	—	1.30	—	ns
		LFE2M50	1.20	—	1.40	—	1.60	—	ns
		LFE2M70	1.20	—	1.40	—	1.60	—	ns
		LFE2M100	1.20	—	1.40	—	1.60	—	ns
t_{SU_DELE}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFE2-6	1.00	—	1.30	—	1.60	—	ns
		LFE2-12	1.00	—	1.30	—	1.60	—	ns
		LFE2-20	1.00	—	1.30	—	1.60	—	ns
		LFE2-35	1.00	—	1.30	—	1.60	—	ns
		LFE2-50	1.00	—	1.30	—	1.60	—	ns
		LFE2-70	1.00	—	1.30	—	1.60	—	ns
		LFE2M20	1.20	—	1.60	—	1.90	—	ns
		LFE2M35	1.20	—	1.60	—	1.90	—	ns
		LFE2M50	1.20	—	1.60	—	1.90	—	ns
		LFE2M70	1.20	—	1.60	—	1.90	—	ns
		LFE2M100	1.20	—	1.60	—	1.90	—	ns

LatticeECP2/M External Switching Characteristics[9] (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7 Min.	-7 Max.	-6 Min.	-6 Max.	-5 Min.	-5 Max.	Units
t_{H_DELE}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
f_{MAX_IOE}	Clock Frequency of I/O and PFU Register	ECP2/M	—	420	—	357	—	311	MHz
General I/O Pin Parameters (using Primary Clock with PLL)[1]									
t_{COPLL}[10]	Clock to Output - PIO Output Register	LFE2-6	—	2.30	—	2.60	—	2.80	ns
		LFE2-12	—	2.30	—	2.60	—	2.80	ns
		LFE2-20	—	2.30	—	2.60	—	2.80	ns
		LFE2-35	—	2.30	—	2.60	—	2.80	ns
		LFE2-50	—	2.30	—	2.60	—	2.80	ns
		LFE2-70	—	2.30	—	2.60	—	2.80	ns
		LFE2M20	—	2.30	—	2.60	—	2.80	ns
		LFE2M35	—	2.30	—	2.60	—	2.80	ns
		LFE2M50	—	2.60	—	2.90	—	3.10	ns
		LFE2M70	—	2.60	—	2.90	—	3.10	ns
		LFE2M100	—	2.70	—	3.00	—	3.20	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	LFE2-6	0.70	—	0.80	—	0.90	—	ns
		LFE2-12	0.70	—	0.80	—	0.90	—	ns
		LFE2-20	0.70	—	0.80	—	0.90	—	ns
		LFE2-35	0.70	—	0.80	—	0.90	—	ns
		LFE2-50	0.70	—	0.80	—	0.90	—	ns
		LFE2-70	0.70	—	0.80	—	0.90	—	ns
		LFE2M20	0.70	—	0.80	—	0.90	—	ns
		LFE2M35	0.70	—	0.80	—	0.90	—	ns
		LFE2M50	0.70	—	0.80	—	0.90	—	ns
		LFE2M70	0.70	—	0.80	—	0.90	—	ns
		LFE2M100	0.80	—	0.90	—	1.00	—	ns

LatticeECP2/M External Switching Characteristics[9] (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7 Min.	-7 Max.	-6 Min.	-6 Max.	-5 Min.	-5 Max.	Units
t_{HPLL}	Clock to Data Hold - PIO Input Register	LFE2-6	1.00	—	1.20	—	1.40	—	ns
		LFE2-12	1.00	—	1.20	—	1.40	—	ns
		LFE2-20	1.00	—	1.20	—	1.40	—	ns
		LFE2-35	1.00	—	1.20	—	1.40	—	ns
		LFE2-50	1.00	—	1.20	—	1.40	—	ns
		LFE2-70	1.00	—	1.20	—	1.40	—	ns
		LFE2M20	1.00	—	1.20	—	1.40	—	ns
		LFE2M35	1.00	—	1.20	—	1.40	—	ns
		LFE2M50	1.00	—	1.20	—	1.40	—	ns
		LFE2M70	1.00	—	1.20	—	1.40	—	ns
		LFE2M100	1.00	—	1.20	—	1.40	—	ns
t_{SU_DELPLL}	Clock to Data Setup - PIO Input Register with Data Input Delay	LFE2-6	1.80	—	2.00	—	2.20	—	ns
		LFE2-12	1.80	—	2.00	—	2.20	—	ns
		LFE2-20	1.80	—	2.00	—	2.20	—	ns
		LFE2-35	1.80	—	2.00	—	2.20	—	ns
		LFE2-50	1.80	—	2.00	—	2.20	—	ns
		LFE2-70	1.80	—	2.00	—	2.20	—	ns
		LFE2M20	1.80	—	2.00	—	2.20	—	ns
		LFE2M35	1.80	—	2.00	—	2.20	—	ns
		LFE2M50	1.90	—	2.10	—	2.30	—	ns
		LFE2M70	1.90	—	2.10	—	2.30	—	ns
		LFE2M100	2.00	—	2.20	—	2.40	—	ns
t_{H_DELPLL}	Clock to Data Hold - PIO Input Register with Input Data Delay	LFE2-6	0.00	—	0.00	—	0.00	—	ns
		LFE2-12	0.00	—	0.00	—	0.00	—	ns
		LFE2-20	0.00	—	0.00	—	0.00	—	ns
		LFE2-35	0.00	—	0.00	—	0.00	—	ns
		LFE2-50	0.00	—	0.00	—	0.00	—	ns
		LFE2-70	0.00	—	0.00	—	0.00	—	ns
		LFE2M20	0.00	—	0.00	—	0.00	—	ns
		LFE2M35	0.00	—	0.00	—	0.00	—	ns
		LFE2M50	0.00	—	0.00	—	0.00	—	ns
		LFE2M70	0.00	—	0.00	—	0.00	—	ns
		LFE2M100	0.00	—	0.00	—	0.00	—	ns
DDR I/O Pin Parameters[2]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	ECP2/M	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	ECP2/M	0.640	—	0.640	—	0.640	—	UI
t_{DQVBS}	Data Valid Before DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
t_{DQVAS}	Data Valid After DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
f_{MAX_DDR}	DDR Clock Frequency[6]	ECP2/M	95	200	95	166	95	133	MHz
DDR2 I/O Pin Parameters[3]									
t_{DVADQ}	Data Valid After DQS (DDR Read)	ECP2/M	—	0.225	—	0.225	—	0.225	UI
t_{DVEDQ}	Data Hold After DQS (DDR Read)	ECP2/M	0.640	—	0.640	—	0.640	—	UI

LatticeECP2/M External Switching Characteristics[9] (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7 Min.	-7 Max.	-6 Min.	-6 Max.	-5 Min.	-5 Max.	Units
t_{DQVBS}	Data Valid Before DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
t_{DQVAS}	Data Valid After DQS (DDR Write)	ECP2/M	0.250	—	0.250	—	0.250	—	UI
f_{MAX_DDR2}	DDR Clock Frequency	ECP2/M	133	266	133	200	133	166	MHz
SPI4.2 I/O Pin Parameters Static Alignment[4, 8, 11]									
		ECP2-20	—	750	—	622	—	622	Mbps
		ECP2-35	—	750	—	622	—	622	Mbps
		ECP2-50	—	750	—	622	—	622	Mbps
		ECP2-70	—	750	—	622	—	622	Mbps
	Maximum Data Rate	ECP2M20	—	622	—	622	—	622	Mbps
		ECP2M35	—	622	—	622	—	622	Mbps
		ECP2M50	—	622	—	622	—	622	Mbps
		ECP2M70	—	622	—	622	—	622	Mbps
		ECP2M100	—	622	—	622	—	622	Mbps
		ECP2-20	—	0.25	—	0.25	—	0.25	UI
		ECP2-35	—	0.25	—	0.25	—	0.25	UI
		ECP2-50	—	0.25	—	0.25	—	0.25	UI
		ECP2-70	—	0.25	—	0.25	—	0.25	UI
$t_{DVACLKSPI}$	Data Valid After CLK (Receive)	ECP2M20	—	0.21	—	0.21	—	0.21	UI
		ECP2M35	—	0.21	—	0.21	—	0.21	UI
		ECP2M50	—	0.21	—	0.21	—	0.21	UI
		ECP2M70	—	0.21	—	0.21	—	0.21	UI
		ECP2M100	—	0.21	—	0.21	—	0.21	UI
		ECP2-20	0.75	—	0.75	—	0.75	—	UI
		ECP2-35	0.75	—	0.75	—	0.75	—	UI
		ECP2-50	0.75	—	0.75	—	0.75	—	UI
		ECP2-70	0.75	—	0.75	—	0.75	—	UI
$t_{DVECLKSPI}$	Data Hold After CLK (Receive)	ECP2M20	0.79	—	0.79	—	0.79	—	UI
		ECP2M35	0.79	—	0.79	—	0.79	—	UI
		ECP2M50	0.79	—	0.79	—	0.79	—	UI
		ECP2M70	0.79	—	0.79	—	0.79	—	UI
		ECP2M100	0.79	—	0.79	—	0.79	—	UI
		ECP2-20	—	280	—	280	—	280	ps
		ECP2-35	—	280	—	280	—	280	ps
		ECP2-50	—	280	—	280	—	280	ps
		ECP2-70	—	280	—	280	—	280	ps
t_{DIASPI}	Data Invalid After Clock (Transmit)	ECP2M20	—	230	—	230	—	230	ps
		ECP2M35	—	230	—	230	—	230	ps
		ECP2M50	—	230	—	230	—	230	ps
		ECP2M70	—	230	—	230	—	230	ps
		ECP2M100	—	230	—	230	—	230	ps

LatticeECP2/M External Switching Characteristics[9] (Continued)

Over Recommended Operating Conditions

Parameter	Description	Device	-7 Min.	-7 Max.	-6 Min.	-6 Max.	-5 Min.	-5 Max.	Units
t_{DIBSPI}	Data Invalid Before Clock (Transmit)	ECP2-20	—	280	—	280	—	280	ps
		ECP2-35	—	280	—	280	—	280	ps
		ECP2-50	—	280	—	280	—	280	ps
		ECP2-70	—	280	—	280	—	280	ps
		ECP2M20	—	230	—	230	—	230	ps
		ECP2M35	—	230	—	230	—	230	ps
		ECP2M50	—	230	—	230	—	230	ps
		ECP2M70	—	230	—	230	—	230	ps
		ECP2M100	—	230	—	230	—	230	ps
XGMII I/O Pin Parameters (312 Mbps)[5]									
$t_{SUXGMII}$	Data Setup Before Read Clock	ECP2/M	480	—	480	—	480	—	ps
t_{HXGMII}	Data Hold After Read Clock	ECP2/M	480	—	480	—	480	—	ps
$t_{DVBCKXGMII}$	Data Valid Before Clock	ECP2/M	960	—	960	—	960	—	ps
$t_{DVACKXGMII}$	Data Valid After Clock	ECP2/M	960	—	960	—	960	—	ps
Primary									
f_{MAX_PRI}[7]	Frequency for Primary Clock Tree	ECP2/M	—	420	—	357	—	311	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Bank	ECP2/M	—	300	—	360	—	420	ps
Edge Clock									
f_{MAX_EDGE}[7]	Frequency for Edge Clock	ECP2/M	—	420	—	357	—	311	MHz
t_{W_EDGE}	Clock Pulse Width for Edge Clock	ECP2/M	0.95	—	1.19	—	2.00	—	ns
t_{SKEW_EDGE}	Edge Clock Skew Within an Edge of the Device	ECP2/M	—	300	—	360	—	420	ps

1. General timing numbers based on LVCMOS 2.5, 12mA, 0pf load.
2. DDR timing numbers based on SSTL25 for BGA packages only.
3. DDR2 timing numbers based on SSTL18 for BGA packages only.
4. SPI4.2 and SFI4 timing numbers based on LVDS25 for BGA packages only.
5. XGMII timing numbers based on HSTL class I. A corresponding left/right dedicated clock buffer is used when using the SPI4.2 interface to the left or right edge of the device. For SPI4.2 mode, the software tool will help in selecting the appropriate clock buffer.
6. IP will be used to support DDR and DDR2 memory data rates down to 95MHz. This approach uses a free-running clock and PFU register to sample the data instead of the hardwired DDR memory interface.
7. Using the LVDS I/O standard.
8. ECP2-6 and ECP2-12 do not support SPI4.2
9. The AC numbers do not apply to PCLK6 and PCLK7.
10. Applies to CLKOP only.
11. Please refer to TN1159, LatticeECP2/M Pin Assignment Recommendations for best performance.

Timing v.A 0.11

LatticeECP2/M Internal Switching Characteristics[1]

Over Recommended Operating Conditions

Parameter	Description	-7 Min.	-7 Max.	-6 Min.	-6 Max.	-5 Min.	-5 Max.	Units
PFU/PFF Logic Mode Timing								
t_{LUT4_PFU}	LUT4 delay (A to D inputs to F output)	—	0.180	—	0.198	—	0.216	ns
t_{LUT6_PFU}	LUT6 delay (A to D inputs to OFX output)	—	0.304	—	0.331	—	0.358	ns
t_{LSR_PFU}	Set/Reset to output of PFU (Asynchronous)	—	0.600	—	0.655	—	0.711	ns
t_{SUM_PFU}	Clock to Mux (M0,M1) Input Setup Time	0.128	—	0.129	—	0.129	—	ns
t_{HM_PFU}	Clock to Mux (M0,M1) Input Hold Time	-0.051	—	-0.049	—	-0.046	—	ns
t_{SUD_PFU}	Clock to D input setup time	0.061	—	0.071	—	0.081	—	ns
t_{HD_PFU}	Clock to D input hold time	0.002	—	0.003	—	0.003	—	ns
t_{CK2Q_PFU}	Clock to Q delay, (D-type Register Configuration)	—	0.285	—	0.309	—	0.333	ns
PFU Dual Port Memory Mode Timing								
t_{CORAM_PFU}	Clock to Output (F Port)	—	0.902	—	1.083	—	1.263	ns
t_{SUDATA_PFU}	Data Setup Time	-0.172	—	-0.205	—	-0.238	—	ns
t_{HDATA_PFU}	Data Hold Time	0.199	—	0.235	—	0.271	—	ns
t_{SUADDR_PFU}	Address Setup Time	-0.245	—	-0.284	—	-0.323	—	ns
t_{HADDR_PFU}	Address Hold Time	0.246	—	0.285	—	0.324	—	ns
t_{SUWREN_PFU}	Write/Read Enable Setup Time	-0.122	—	-0.145	—	-0.168	—	ns
t_{HWREN_PFU}	Write/Read Enable Hold Time	0.132	—	0.156	—	0.180	—	ns
PIC Timing								
PIO Input/Output Buffer Timing								
t_{IN_PIO}	Input Buffer Delay (LVCMOS25)	—	0.613	—	0.681	—	0.749	ns
t_{OUT_PIO}	Output Buffer Delay (LVCMOS25)	—	1.115	—	1.115	—	1.343	ns
IOLOGIC Input/Output Timing								
t_{SUI_PIO}	Input Register Setup Time (Data Before Clock)	0.596	—	0.645	—	0.694	—	ns
t_{HI_PIO}	Input Register Hold Time (Data after Clock)	-0.570	—	-0.614	—	-0.658	—	ns
t_{COO_PIO}	Output Register Clock to Output Delay	—	0.61	—	0.66	—	0.72	ns
t_{SUCE_PIO}	Input Register Clock Enable Setup Time	0.032	—	0.037	—	0.041	—	ns
t_{HCE_PIO}	Input Register Clock Enable Hold Time	-0.022	—	-0.025	—	-0.028	—	ns
t_{SULSR_PIO}	Set/Reset Setup Time	0.184	—	0.201	—	0.217	—	ns
t_{HLSR_PIO}	Set/Reset Hold Time	-0.080	—	-0.086	—	-0.093	—	ns
EBR Timing								
t_{CO_EBR}	Clock (Read) to output from Address or Data	—	2.51	—	2.75	—	2.99	ns
t_{COO_EBR}	Clock (Write) to output from EBR output Register	—	0.33	—	0.36	—	0.39	ns
t_{SUDATA_EBR}	Setup Data to EBR Memory	-0.157	—	-0.181	—	-0.205	—	ns
t_{HDATA_EBR}	Hold Data to EBR Memory	0.173	—	0.195	—	0.217	—	ns
t_{SUADDR_EBR}	Setup Address to EBR Memory	-0.115	—	-0.130	—	-0.145	—	ns
t_{HADDR_EBR}	Hold Address to EBR Memory	0.138	—	0.155	—	0.172	—	ns
t_{SUWREN_EBR}	Setup Write/Read Enable to PFU Memory	-0.128	—	-0.149	—	-0.170	—	ns

LatticeECP2/M Internal Switching Characteristics[1] (Continued)

Over Recommended Operating Conditions

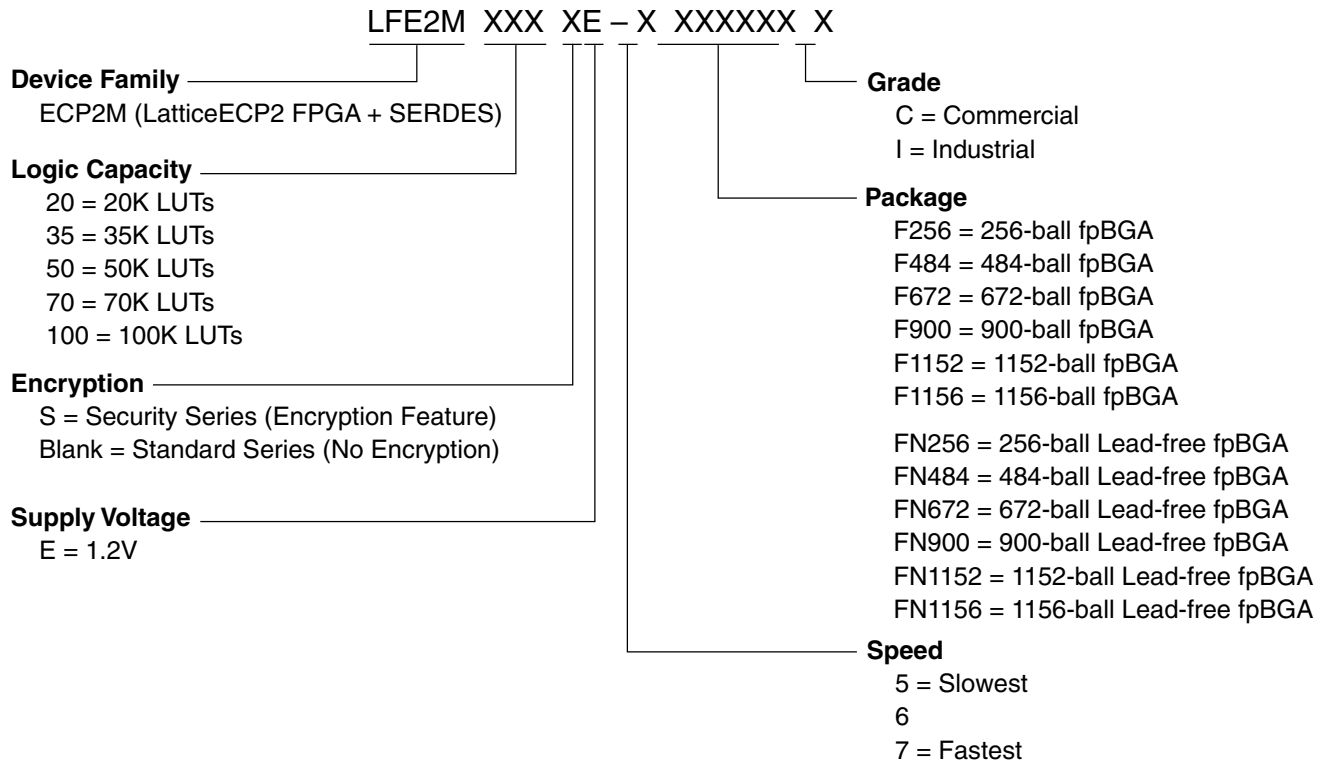| Parameter	Description	-7 Min.	-7 Max.	-6 Min.	-6 Max.	-5 Min.	-5 Max.	Units
t$_{HWREN\_EBR}$	Hold Write/Read Enable to PFU Memory	0.139	—	0.156	—	0.173	—	ns
t$_{SUCE\_EBR}$	Clock Enable Setup Time to EBR Output Register	0.123	—	0.134	—	0.145	—	ns
t$_{HCE\_EBR}$	Clock Enable Hold Time to EBR Output Register	-0.081	—	-0.090	—	-0.100	—	ns
t$_{RSTO\_EBR}$	Reset To Output Delay Time from EBR Output Register	—	1.03	—	1.15	—	1.26	ns
t$_{SUBE\_EBR}$	Byte Enable Set-Up Time to EBR Output Register	-0.115	—	-0.130	—	-0.145	—	ns
t$_{HBE\_EBR}$	Byte Enable Hold Time to EBR Output Register	0.138	—	0.155	—	0.172	—	ns
GPLL Parameters								
t$_{RSTREC\_GPLL}$	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
SPLL Parameters								
t$_{RSTREC\_SPLL}$	Reset Recovery to Rising Clock	1.00	—	1.00	—	1.00	—	ns
DSP Block Timing[2,3]								
t$_{SUI\_DSP}$	Input Register Setup Time	0.12	—	0.13	—	0.14	—	ns
t$_{HI\_DSP}$	Input Register Hold Time	0.02	—	-0.01	—	-0.03	—	ns
t$_{SUP\_DSP}$	Pipeline Register Setup Time	2.18	—	2.42	—	2.66	—	ns
t$_{HP\_DSP}$	Pipeline Register Hold Time	-0.68	—	-0.77	—	-0.86	—	ns
t$_{SUO\_DSP}$	Output Register Setup Time	4.26	—	4.71	—	5.16	—	ns
t$_{HO\_DSP}$	Output Register Hold Time	-1.25	—	-1.40	—	-1.54	—	ns
t$_{COI\_DSP}$	Input Register Clock to Output Time	—	3.92	—	4.30	—	4.68	ns
t$_{COP\_DSP}$	Pipeline Register Clock to Output Time	—	1.87	—	1.98	—	2.08	ns
t$_{COO\_DSP}$	Output Register Clock to Output Time	—	0.50	—	0.52	—	0.55	ns
t$_{SUADDSUB}$	AddSub Input Register Setup Time	-0.24	—	-0.26	—	-0.28	—	ns
t$_{HADDSUB}$	AddSub Input Register Hold Time	0.27	—	0.29	—	0.32	—	ns

1. Internal parameters are characterized but not tested on every device.
2. These parameters apply to LatticeECP devices only.
3. DSP Block is configured in Multiply Add/Sub 18x18 Mode.

Timing v.A 0.11

LatticeECP2M Part Number Description

LFE2M XXX XE – X XXXXXX X

Device Family
ECP2M (LatticeECP2 FPGA + SERDES)

Logic Capacity
20 = 20K LUTs
35 = 35K LUTs
50 = 50K LUTs
70 = 70K LUTs
100 = 100K LUTs

Encryption
S = Security Series (Encryption Feature)
Blank = Standard Series (No Encryption)

Supply Voltage
E = 1.2V

Grade
C = Commercial
I = Industrial

Package
F256 = 256-ball fpBGA
F484 = 484-ball fpBGA
F672 = 672-ball fpBGA
F900 = 900-ball fpBGA
F1152 = 1152-ball fpBGA
F1156 = 1156-ball fpBGA

FN256 = 256-ball Lead-free fpBGA
FN484 = 484-ball Lead-free fpBGA
FN672 = 672-ball Lead-free fpBGA
FN900 = 900-ball Lead-free fpBGA
FN1152 = 1152-ball Lead-free fpBGA
FN1156 = 1156-ball Lead-free fpBGA

Speed
5 = Slowest
6
7 = Fastest

Ordering Information

Note: LatticeECP2M devices are dual marked. For example, the commercial speed grade LFE2M50E-7F672C is also marked with industrial grade -6I (LFE2M50E-6F672I). The commercial grade is one speed grade faster than the associated dual mark industrial grade. The slowest commercial grade does not have industrial markings. The markings appear as follows:

Lattice
ECP2M
LFE2M35E
7F672C-6I

Datecode

Lattice
ECP2M
LFE2M35SE
7F672C-6I

Datecode
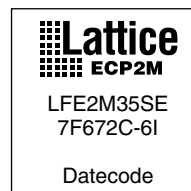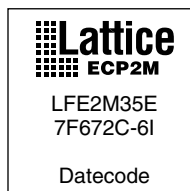
Contact Your Local Lattice Sales Representative for Product Availability.

LatticeECP2M Standard Series Devices, Lead-Free Packaging

Commercial

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M20E-5FN484C	304	1.2V	-5	Lead-Free fpBGA	484	COM	20
LFE2M20E-6FN484C	304	1.2V	-6	Lead-Free fpBGA	484	COM	20
LFE2M20E-7FN484C	304	1.2V	-7	Lead-Free fpBGA	484	COM	20
LFE2M20E-5FN256C	140	1.2V	-5	Lead-Free fpBGA	256	COM	20
LFE2M20E-6FN256C	140	1.2V	-6	Lead-Free fpBGA	256	COM	20
LFE2M20E-7FN256C	140	1.2V	-7	Lead-Free fpBGA	256	COM	20

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M35E-5FN672C	410	1.2V	-5	Lead-Free fpBGA	672	COM	35
LFE2M35E-6FN672C	410	1.2V	-6	Lead-Free fpBGA	672	COM	35
LFE2M35E-7FN672C	410	1.2V	-7	Lead-Free fpBGA	672	COM	35
LFE2M35E-5FN484C	303	1.2V	-5	Lead-Free fpBGA	484	COM	35
LFE2M35E-6FN484C	303	1.2V	-6	Lead-Free fpBGA	484	COM	35
LFE2M35E-7FN484C	303	1.2V	-7	Lead-Free fpBGA	484	COM	35
LFE2M35E-5FN256C	140	1.2V	-5	Lead-Free fpBGA	256	COM	35
LFE2M35E-6FN256C	140	1.2V	-6	Lead-Free fpBGA	256	COM	35
LFE2M35E-7FN256C	140	1.2V	-7	Lead-Free fpBGA	256	COM	35

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M50E-5FN900C	410	1.2V	-5	Lead-Free fpBGA	900	COM	50
LFE2M50E-6FN900C	410	1.2V	-6	Lead-Free fpBGA	900	COM	50
LFE2M50E-7FN900C	410	1.2V	-7	Lead-Free fpBGA	900	COM	50
LFE2M50E-5FN672C	372	1.2V	-5	Lead-Free fpBGA	672	COM	50
LFE2M50E-6FN672C	372	1.2V	-6	Lead-Free fpBGA	672	COM	50
LFE2M50E-7FN672C	372	1.2V	-7	Lead-Free fpBGA	672	COM	50
LFE2M50E-5FN484C	270	1.2V	-5	Lead-Free fpBGA	484	COM	50
LFE2M50E-6FN484C	270	1.2V	-6	Lead-Free fpBGA	484	COM	50
LFE2M50E-7FN484C	270	1.2V	-7	Lead-Free fpBGA	484	COM	50

Part Number	I/Os	Voltage	Grade	Package	Pins	Temp.	LUTs (K)
LFE2M70E-5FN1152C	436	1.2V	-5	Lead-Free fpBGA	1152	COM	70
LFE2M70E-6FN1152C	436	1.2V	-6	Lead-Free fpBGA	1152	COM	70
LFE2M70E-7FN1152C	436	1.2V	-7	Lead-Free fpBGA	1152	COM	70
LFE2M70E-5FN900C	416	1.2V	-5	Lead-Free fpBGA	900	COM	70
LFE2M70E-6FN900C	416	1.2V	-6	Lead-Free fpBGA	900	COM	70
LFE2M70E-7FN900C	416	1.2V	-7	Lead-Free fpBGA	900	COM	70